05/17/03

My dear fellow Semiconductor Engineers,

When chemist Gordon Moore first published his article [1] where he plotted a chart of the "*log of the components per integrated function*" which doubled every year, no one understood the vertical axis label "*Integrated Function.*" And no one had any idea that this speculation based on numbers "pulled out of a hat" would be important to the future development of semiconductor industry.

I remember when I read the article; that the article was written with very vague language and with a cartoon about cosmetics and a computer. There was no reference to where the numbers came from, and the chart did not contain already established numbers such as Last, Haas, and Kattner's very first Fairchild planar integrated circuits which contained six components and was demonstrated in November 1960. One of Fairchild's 1963 Micrologic elements (half shift register), designed by Norman and Anderson, had 48 elements, and should have set the "number of" components in 1975 to 196,608, not 65,000 as Moore predicted. This really does not matter, because the chart never fit data in the first place anyway. When Intel introduced the 8080 in 1975, the number of transistors was just below 5000. In the coordinate system Moore chose ($\log_2$ – lin), even if the numbers changed by 100%, they still look to the eye as a reasonable fit to a straight line.

When I looked at the bottom of the page of Moore's article, I saw: 'Electronics, April 1965.' I thought the article was one of the editors April Fool jokes, and I quickly forgot about the article.

I started to pay attention to the article many years later when Moore's observation, suddenly become "Law," and I paid even more attention when "Moore's Law" became the doctrine of advanced semiconductor companies.

Let's for a moment pretend that the "Law" is Law and we will follow it. According to the data G. Moore presented at last February's ISSCC [2], both Intel's update and the ITRS 2001 roadmap will reach a feature size of 400 Å around 2010 (Fig. 1). If this trend is correct, the 128 Giga DRAM will have a feature size of 400 Å and die size approximately 40 x 90 mm. If we assume that production will be done on 300 mm wafers with 100% yield, each wafer will have 12 die. From the past we know, that typically ten months after product introduction, prices dropped by 50%. If we assume that trend extrapolates, then, in 2010 a semiconductor manufacturer will spend roughly $3-4 billion on a manufacturing Fab, $1-2 million on a mask set, pay a premium for 300 mm starting material, and produce 12 dice per wafer which will be selling for a few dollars. Sounds like nonsense? It not only sounds like nonsense, it is.

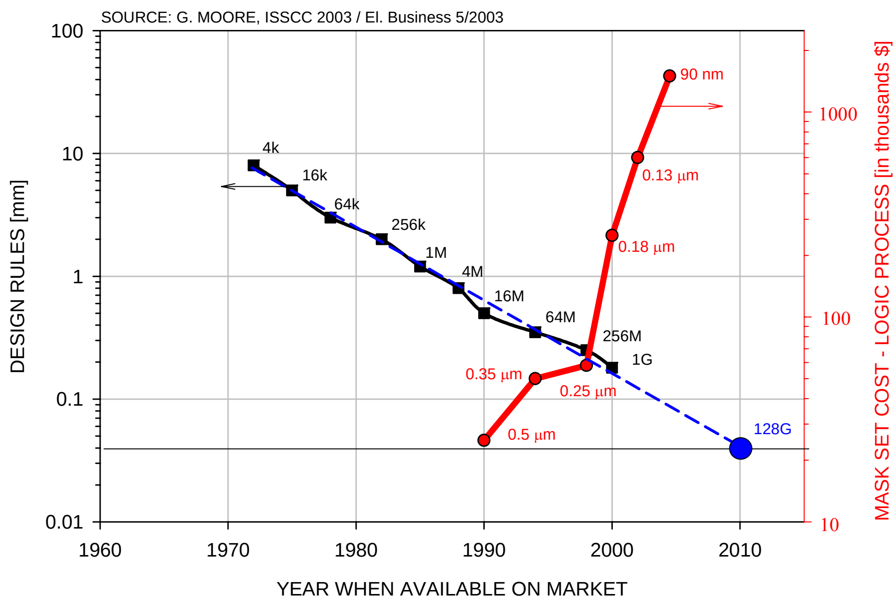

Fig. 1. Minimum Feature Size (Data from [2])

Compare the 128 Giga DRAM or equivalent logic products from another point of view. The butterfly, whose brain's processing capabilities are estimated by biologists to be at most equivalent to 2 or 3 bit microcontroller, has a wing features in deep-submicron scale for centuries (Fig. 2). A butterfly is able to perform 3-D flight control, real-time pattern recognition, and duplicate itself with a typical yield 300-400%.

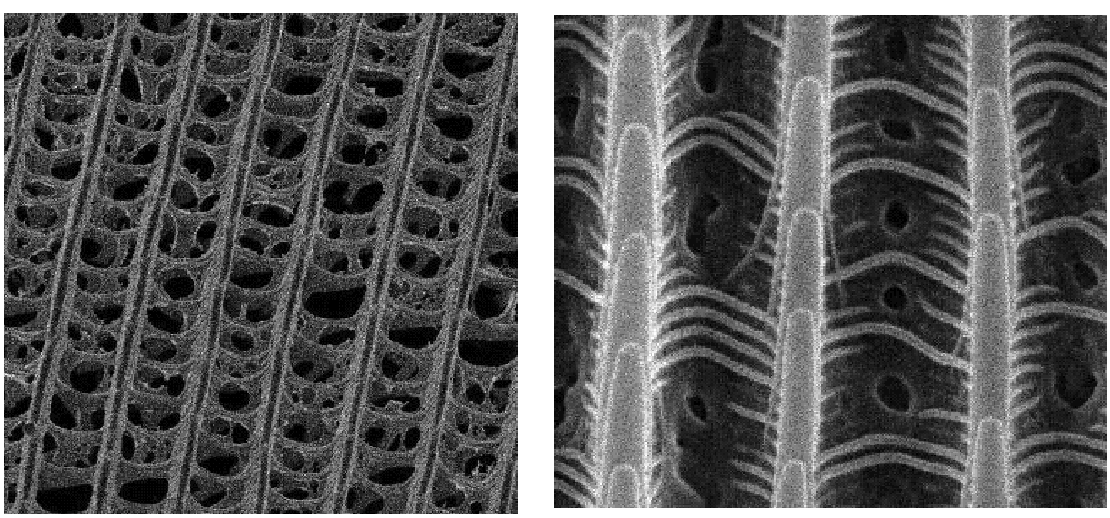

Fig. 2. SEM photograph of butterfly wing: Left) Stacked structure corresponds to bit lines (vertical) with multi-layered word lines (horizontal). Right) the approximately 500 A diameter plugs are connecting multi-layered cells.

If you still think that this is not enough functionality for a 3 bit controller, consider that the butterfly, through extremely sophisticated radiation exchange between different layers of his wing, change the colors of his wing in the UV region to signal to other butterflies that it is ready for sex.

The “Law” may have some sense for Intel microprocessor products where each generation increases die size and transistor count. However, there is and always will be, a large class of microelectronics products which require only small die and for economical reasons is better produced them by low cost technology with a small diameter wafers. For example, in the ASIC business there are products that run in several large batches for 3 to 4 months, and then they are never produced again. Two hundred mm wafers with cheaper production technology are perfectly justified in such cases. Another example is the very successful Microchip. They recently shipped their 2 billionth microcontroller which was produced with relatively low-tech processing technology. Not every product in the future will need 6 layers of copper, high and low k materials, and advanced photolithography which only the top ten manufacturers can afford.

What is wrong with 200 mm wafer production and why is it that somebody who uses common sense cannot go in this direction? The reason is very simple: The International Sematech, SEMI, and SRC are under the control of a few manufacturers who are pushing the manufacturers of semiconductor equipment into developing tools for their needs. To illustrate the situation, consider Applied Materials. My company, Microchip, National, Analog Devices, LSI Logic and similar small or medium size companies form a significant customer base for Applied Materials. However, because the cost of development of new tools for new processes following “Moore’s Law” is so expensive and time consuming, companies like Applied cannot continue the development of 200 mm tools. In reality, small and medium-size companies are subsidizing through purchasing of tools from Applied, the development cost of a new generation tools which they will not be able to afford later. Applied decided that new tools will be developed only in 300 mm version, and already single-wafer wet-cleaning tools exists only in a 300 mm version, with no plans to extend production to smaller wafer diameter. This situation is similar with other equipment vendors. Is this a bad decision on the part of the equipment manufacturer? Of course not, they have no other choice if they want to stay in business.

One of the solutions to this problem is very simple. Let’s establish a new law where the technical progress is balanced with economic values.
Gordon Moore suggested at the end of his 2003 ISSCC presentation that we should “delay forever” the end of his prediction. Unfortunately, the semiconductor business is not only about scaling of devices, but also about money, or to be more explicit – it is only about money. In everything where money is involved there is no “delay” and absolutely no “forever.” The sooner we learn more from butterflies and forget about “Moore’s Law,” the sooner the semiconductor business will be better off.

[1] G.E. Moore, “Cramming more components onto integrated circuits,” Electronics, Vol. 38 (1965), April 15
[2] G.E. Moore, “No exponential is forever,” IEEE ISSCC, February 2003

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